REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add CAGE number 34335 as approved source for 01 device. Add CAGE number 66579 for devices 01 through 04. Add device 04. Delete footnote 4/ from t_{QLQV} condition block. Add footnote 4/ to t_{EHQZ} condition block. Remove test condition C. Make editorial changes to margin test method B. Make editorial changes to power dissipation.	89-08-23	M.A. Frye
B	Add case outline letter and device type 05 for vendor CAGE number 1FN41. Add test condition C to 4.2 and 4.3.2. Add vendor CAGE number 34649 to the drawing as a source for device types 01XX, 02XX, and 03XX. Add vendor CAGE 34335 for devices 04XX, 04YX, 05XX, and 05YX. Removed vendor CAGE number 60991 from drawing. Editorial changes throughout.	93-02-02	M.A. Frye
C	Make changes to paragraph 1.3, Table I, and AC waveforms. Add paragraph 3.11 and remove paragraph 4.2c. Updated boilerplate and Source Approval Bulletin.	96-03-01	M.A. Frye

REV																			
SHEET																			
REV																			
SHEET																			

REV STATUS OF SHEETS															
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13		

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
Ray Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88-06-13

REVISION LEVEL
C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, MEMORY, DIGITAL, CMOS, 64K x 8 UVEPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-87648**

SHEET 1 OF 13

DESC FORM 193
JUL 94

5962-E307-96

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-87648	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01		64K x 8-bit UVEPROM	150 ns
02		64K x 8-bit UVEPROM	200 ns
03		64K x 8-bit UVEPROM	250 ns
04		64K x 8-bit UVEPROM	120 ns
05		64K x 8-bit UVEPROM	90 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line 2/
Y	CQCC1-N32	32	Rectangular leadless chip carrier 2/
Z	See figure 1	32	"J" lead chip carrier 2/

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Storage temperature range . . . . . -65°C to +150°C
Input voltages with respect to ground . . . . . -0.6 V dc to +6.25 V dc
Output voltages with respect to ground . . . . . -0.6 V dc to V_{CC} +1.0 V dc
Voltage on pin A9 with respect to ground . . . . . -0.6 V dc to +13.5 V dc
V_{PP} supply voltage with respect to ground . . . . . -0.6 V dc to +14.0 V dc
Power dissipation (P_D) 3/ . . . . . 350 mW
Lead temperature (soldering, 10 seconds) . . . . . +300°C
Thermal resistance, junction-to-case (Θ_{JC}) . . . . . See MIL-STD-1835
Junction temperature (T_J) . . . . . +150°C

1.4 Recommended operating conditions.

Case operating temperature range (T_C) . . . . . -55°C to +125°C
Supply voltage range (V_{CC}) . . . . . +4.5 V dc to 5.5 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

1/ Generic numbers listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103.
2/ Lid shall be transparent to permit ultraviolet light erasure.
3/ Must withstand the added P_D due to short-circuit test; e.g., I_{OS}.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standardized Military Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.3.1 Unprogrammed or erased devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C inspection (see 4.3), the
devices shall be programmed by the manufacturer prior to test in a checkerboard pattern or equivalent (minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.3.2 Programmed devices. The truth table for programmed devices shall as specified by an attached altered item drawing.

3.2.4 Block diagram(s). The block diagram(s) shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

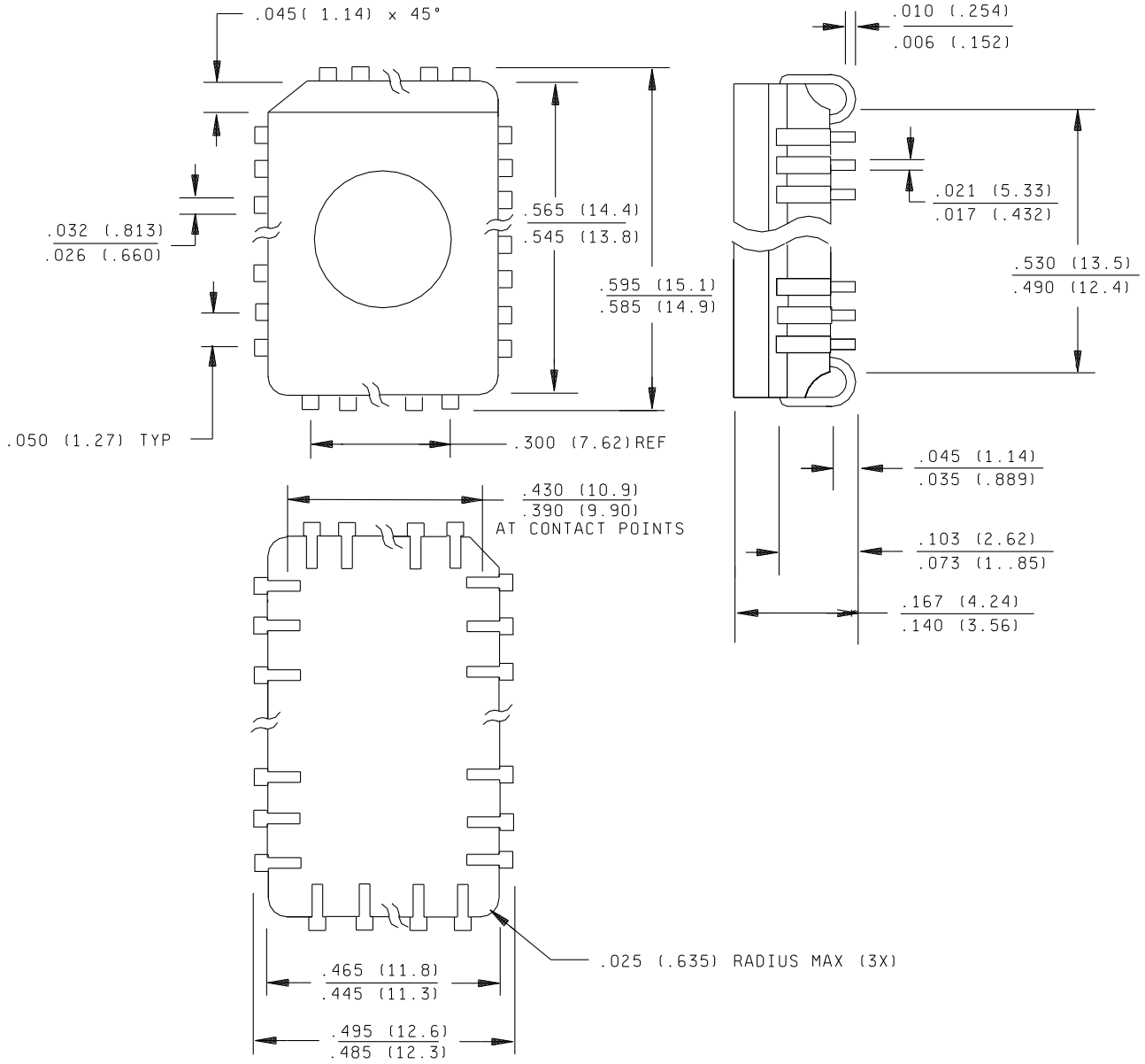
Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ $V_{SS} = 0$ V; 4.5 V $\le V_{CC} \le$ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input leakage current	I_{LI}	V_{IN} = 0 V to 5.5 V	1, 2, 3	All	-10	+10	µA
Output leakage current	I_{LO} 1/	V_{OUT} = 0 V to 5.5 V	1, 2, 3	All	-10	+10	µA
Operating current	I_{CC1}	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$, 0_{0-7} = 0 mA, V_{CC} = 5.5 V f = $1/t_{AVQV}$ (maximum)	1, 2, 3	All		60	mA
Standby current (TTL inputs)	I_{CC2}	$\overline{CE} = V_{IH}$, V_{CC} = 5.5 V	1, 2, 3	All		3	mA
Standby current (CMOS inputs)	I_{CC3}	$\overline{CE} = V_{CC} \pm 0.2$ V, V_{CC} = 5.5 V	1, 2, 3	All		325	µA
Input low voltage (TTL)	V_{IL} 2/ 3/		1, 2, 3	All	-0.1	0.8	V
Input low voltage (CMOS)	V_{IL} 2/ 3/		1, 2, 3	All	-0.2	+0.2	
Input high voltage (TTL)	V_{IH} 2/ 3/		1, 2, 3	All	2.0	V_{CC} + 1.0	
Input high voltage (CMOS)	V_{IH} 2/ 3/		1, 2, 3	All	V_{CC} - 0.2	V_{CC} + 0.2	
Output low voltage	V_{OL}	I_{OL} = 2.1 mA, V_{IL} = 0.8 V, V_{IH} = 2.0 V	1, 2, 3	All		0.45	
Output high voltage	V_{OH}	I_{OH} = -400 µA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	1, 2, 3	All	2.4		V
Output short-circuit	I_{OS}	V_O = 0 V	1, 2, 3	All		±100	mA
Input capacitance (excluding $\overline{OE}/V_{PP}$)	C_{IN1} 4/ 5/	V_{IN} = 0 V, $T_C = +25^\circ C$, f = 1 MHz, see 4.3.1c	4	All		12	pF
Input capacitance (for $\overline{OE}/V_{PP}$)	C_{IN2} 4/ 5/	$\overline{OE}/V_{PP}$ = 0, f = 1 MHz, V_{IN}, V_{OUT} = 0 V, $T_C = +25^\circ C$, see 4.3.1c	4	All		25	pF
Output capacitance	C_{OUT} 4/ 5/	V_{OUT} = 0 V, $T_C = +25^\circ C$, f = 1 MHz, see 4.3.1c	4	All		12	pF
Functional tests		See 4.3.1e	7,8A,8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V; $4.5\ V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Address to output delay	t_{AVQV}	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$ 6/ 7/	9, 10, 11	01		150	ns
				02		200	
				03		250	
				04		120	
				05		90	
$\overline{CE}$ to output delay	t_{ELQV}	$\overline{OE}/V_{PP} = V_{IL}$ 6/ 7/	9, 10, 11	01		150	ns
				02		200	
				03		250	
				04		120	
				05		90	
$\overline{OE}$ to output delay	t_{OLQV}	$\overline{CE} = V_{IL}$ 6/ 7/	9, 10, 11	01		70	ns
				02		75	
				03		100	
				04		50	
				05		40	
$\overline{OE}$ high to output float	t_{EHQZ}	$\overline{CE} = V_{IL}$ 4/ 6/ 7/	9, 10, 11	01		50	ns
				02		55	
				03		60	
				04		45	
				05		30	
Output hold from address $\overline{CE}$ or $\overline{OE}/V_{pp}$ whichever occurred first	t_{AVQZ}	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$ 6/ 7/	9, 10, 11	All	0		ns

1/ Connect all address inputs and $\overline{OE}$ to V_{IH} and measure I_{LO} with the output under test connected to V_{OUT}.
2/ Test for all input and control pins.
3/ Guaranteed if applied as a forcing function for V_{OL} and V_{OH}.
4/ Tested initially and after any design changes that affect this parameter, and therefore shall be guaranteed to the limits specified in table I.
5/ All pins not being tested shall be grounded.
6/ See figure 5.
7/ Equivalent ac test conditions (actual load conditions vary by tester):
Output load = 1 TTL gate and C_L = 100 pF.
Input rise and fall times $\le$ 20 ns.
Input pulse levels: 0.45 V and 2.4 V.
Timing measurement reference levels:
Inputs = 0.8 V and 2.0 V
Outputs = 0.8 V and 2.0 V



NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Metric equivalents are in parentheses.

FIGURE 1. Case outline Z.

Device types	01 through 05	
Case outlines	X	Y and Z
Terminal number	Terminal symbol	
1	A_{15}	NC
2	A_{12}	A_{15}
3	A_7	A_{12}
4	A_6	A_7
5	A_5	A_6
6	A_4	A_5
7	A_3	A_4
8	A_2	A_3
9	A_1	A_2
10	A_O	A_1
11	I/O_0	A_O
12	I/O_1	NC
13	I/O_2	I/O_0
14	GND	I/O_1
15	I/O_3	I/O_2
16	I/O_4	GND
17	I/O_5	NC
18	I/O_6	I/O_3
19	$\underline{I/O}_7$	I/O_4
20	$\overline{CE}$	I/O_5
21	A_{10}	I/O_6
22	$\overline{OE}/V_{PP}$	$\underline{I/O}_7$
23	A_{11}	$\overline{CE}$
24	A_9	A_{10}
25	A_8	$\overline{OE}/V_{PP}$
26	A_{13}	NC
27	A_{14}	A_{11}
28	V_{CC}	A_9
29	---	A_8
30	---	A_{13}
31	---	A_{14}
32	---	V_{CC}

FIGURE 2. Terminal connections - Continued.

Mode	Pins				
	$\overline{CE}$	$\overline{OE}/V_{PP}$	A_9	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X	V_{CC}	D out
Output disable	V_{IL}	V_{IH}	X	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	High Z
Program	V_{IL}	V_{PP}	X	V_{CC} (see note 1)	D in
Program verify	V_{IL}	V_{IL}	X	V_{CC} (see note 1)	D out
Program inhibit	V_{IH}	V_{PP}	X	V_{CC} (see note 1)	High Z
Identity	V_{IL}	V_{IL}	V_H	V_{CC} (see note 1)	Identity code(s)

NOTES:
1. V_{CC} in programming mode shall be as specified by the device manufacturer.
2. V_H = 11.5 V to 12.5 V.
3. X can be either V_{IL} or V_{IH} (don't care state).

FIGURE 3. Truth table.

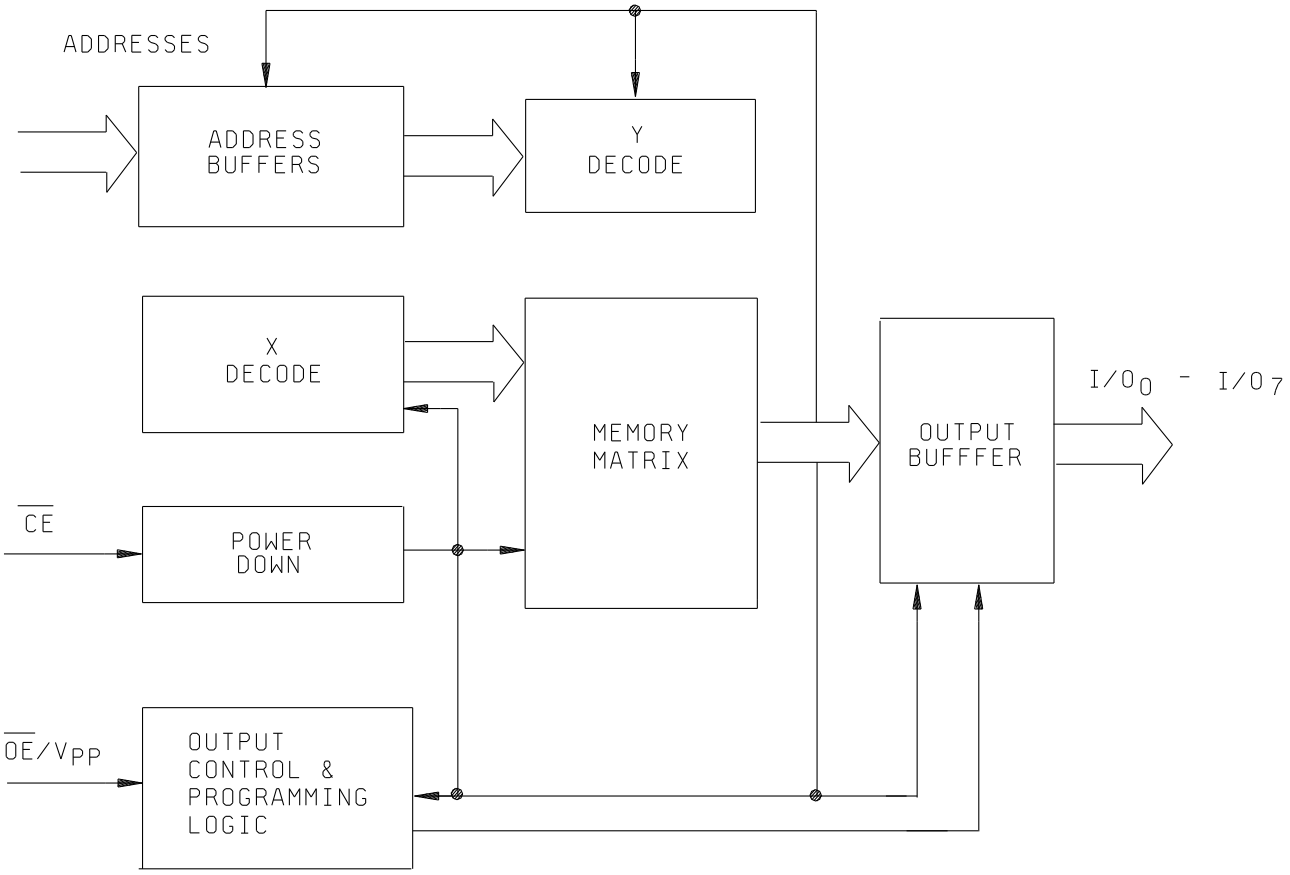
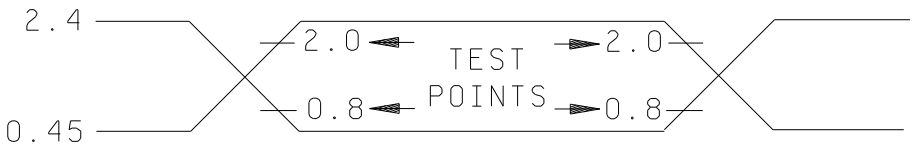


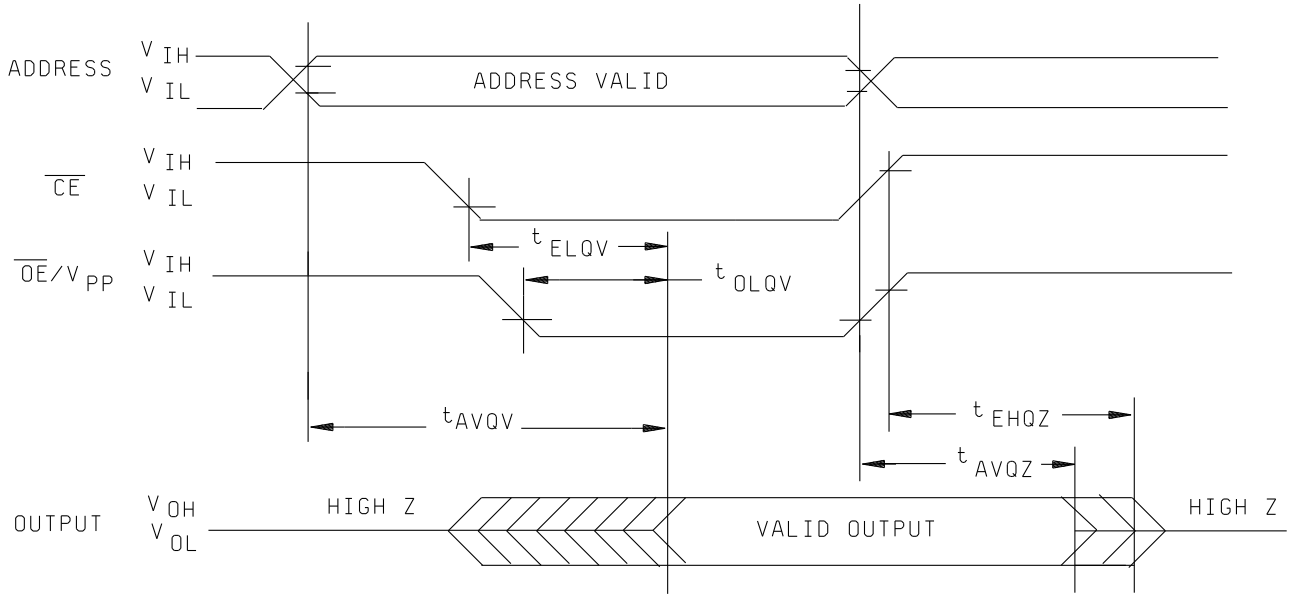
FIGURE 4. Block diagram.

AC testing input, output waveform



AC testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

AC waveforms



NOTES:
1. t_{EHQZ} and t_{AVQZ} are specified from $\overline{OE}/V_{PP}$ or $\overline{CE}$, whichever occurs first.
2. $\overline{OE}/V_{PP}$ may be delayed up to $t_{ELQV} - t_{OLQV}$ after the falling edge of $\overline{CE}$ without impact on t_{ELQV}.

FIGURE 5. Switching waveforms.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing EPROMs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EPROMs. When specified, devices shall be erased in accordance with the procedure and characteristics specified in 4.4 herein.

3.10.2 Programmability of EPROMs. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 herein.

3.10.3 Verification of erasure and/or programmability of EPROMs. When specified devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.11 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process changes which may affect data retention. The methods and procedures may be vendor specific but shall guarantee data retention over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the aquiring or preparing activity, along with test data.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C and D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured for the initial characterization and after any process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. All devices selected for testing shall have the EPROM programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups B, C, and D testing).

e. Subgroups 7 and 8 shall consist of verifying the EPROM pattern specified in 4.3.1d.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test conditions C and D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, those devices that were subjected to a nondestructive subgroup for testing shall be erased and verified.

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for exposure should be a minimum of 15 Ws/cm^2. The erasure time with this dosage is approximately 25 minutes using an ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12000 $\mu W/cm^2$). Exposure of EPROMs to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8,9, 10,11
Group A test requirements (method 5005) 5/	1,2,3,4***,7,8, 9,10**,11**
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8A,8B or 2,8A,10

1/ (*) indicates PDA applies to subgroups 1 and 7.
2/ (**) indicates that subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.
3 (***) see 4.3.1c.
4/ Any subgroups at the same temperature may be combined when using a multifunction tester.
5/ Subgroups 7 and 8 shall consist of verifying the applicable data pattern, see 4.3.1e.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with **MIL-PRF-38535, appendix A.**

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform the Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-03-01

Approved sources of supply for SMD 5962-87648 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/	Replacement military specification PIN
5962-8764801XX	2/ 34335 34649 **2/**	AT27C512R-15DM/883 AM27C512-150/BXA MD27C512-15/B WS27C512L-15DMB	
5962-8764801YX	**2/** 34335 **2/**	AT27C512R-15LM/883 AM27C512-150/BUA WS27C512L-15CMB	
5962-8764801ZX	**2/**	AT27C512R-15KM/883	
5962-8764802XX	01295 **2/** 34335 34649 **2/**	SMJ27C512-20JM AT27C512R-20DM/883 AM27C512-200/BXA MD27C512-20/B WS27C512L-20DMB	
5962-8764802YX	**2/** 34335 **2/**	AT27C512R-20LM/883 AM27C512-200/BUA WS27C512L-20CMB	
5962-8764802ZX	**2/**	AT27C512R-20KLM/883	
5962-8764803XX	01295 **2/** 34335 34649 **2/**	SMJ27C512-25JM AT27C512R-25DM/883 AM27C512-250/BXA MD27C512-25/B WS27C512L-25DMB	
5962-8764803YX	**2/** 34335 **2/**	AT27C512R-25LM/883 AM27C512-250/BUA WS27C512L-25CMB	
5962-8764803ZX	**2/**	AT27C512R-25KM/883	
5962-8764804XX	**2/** **2/** 34335	AT27C512R-12DM/883 WS27C512L-12DMB AM27C512-120/BXA	
5962-8764804YX	**2/** **2/** 34335	AT27C512R-12LM/883 WS27C512L-12CMB AM27C512-120/BUA	
5962-8764804ZX	**2/**	AT27C512R-12KM/883	
5962-8764805XX	**2/** 34335	AT27C512R-90DM/883 AM27C512-90/BXA	
5962-8764805YX	**2/** 34335	AT27C512R-90LM/883 AM27C512-90/BUA	
5962-8764805ZX	**2/**	AT27C512R-90KM/883	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ No longer available from an approved source.

Vendor CAGE number	Vendor name and address	Margin test method
01295	Texas Instruments P. O. Box 6448 Midland, TX 79711	C
1FN41	ATMEL Corporation 2095 Ringwood Avenue San Jose, CA 95131	B
34335	Advanced Micro Devices 901 Thompson Place Sunnyvale, CA 94086	A
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051 Point of contact: 5000 W. Chandler Boulevard Chandler, AZ 85226	B
66579	Waferscale Integration, Inc. 47280 Kato Road Fremont, CA 94538	B

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